Experimental Comparison of MOSFET and JFET 1.1μm Pitch Jots in 1Mjot Stacked BSI Quanta Image Sensors

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***Abstract*— This paper reports on the design, characterization, and comparison of MOSFET and (for the first time) JFET-based QIS readout. Each type of specialized pixel (or "jot") was realized in a 1Mjot array, and 20 different 1Mjot arrays were fabricated together on one stacked BSI chip (20Mjot total).**

I. Introduction

The quanta image sensor (QIS) was proposed in 2005 [1, 2]. A QIS may contain hundreds of millions to billions of specialized pixels, called "jot". The jots detect the number of incident photons and output single-bit or multi-bit counting signal. The QIS image can then be created from jot data by image processing.

The read noise of an image sensor determines its capability of photoelectron counting. Deep sub-electron read noise (DSERN) is required for photoelectron counting [3], corresponding to input-referred read noise of 0.5e- r.m.s. or lower. To realize accurate photoelectron counting with an ideal counting error rate, read noise of 0.15e- r.m.s. is ultimately desired for QIS applications. In a QIS-type readout circuitry, the in-jot source follower (SF) is the major contributor of read noise. Approaches to eliminating QIS read noise include enhancing the conversion gain (CG) on the floating diffusion (FD) node and reducing the voltage noise from the SF.

The pump-gate jot with tapered reset (TPG) was proposed by our group to enhance the CG of jots to the range of 400μV/e-. In 2015, read noise of 0.22e- r.m.s. was demonstrated with this technique in a small 32x32 test array, and photoelectron counting capability was demonstrated without using avalanche gain at room temperature for the first time [4, 5]. The previous results motivated us to merge the PG jot with the QIS-type readout in a more sophisticated sensor system. To achieve this goal, a prototype chip which contains 20 different 1Mjot arrays was designed and fabricated in TSMC 45nm stacked BSI process. Among the 20 arrays on this chip, different jot designs and readout architectures are tested. For the further reduction of the read noise towards 0.15e- r.m.s., several new jot concepts are implemented based on the previous PG jot design, including a JFET-based in-jot SF and a punch-through reset (PTR) diode to replace the reset FET. Thus, a best-case read noise of 0.17e- r.m.s. was demonstrated. In this paper, the characterization results of MOSFET and JFET jots with and without PTR will be discussed and compared.

II. Jot Design and Concept

As mentioned, the QIS read noise can be reduced by improving the CG of the FD and reducing the SF voltage noise. Following the two paths, the following topics are investigated with the prototype chip.

- The comparison of the voltage noise of buried-channel (BC) MOSFET SF and surface-channel (SC) MOSFET SF.
- The improvement of CG by PTR.
- The comparison of the voltage noise of JFET SF and MOSFET SF.
- The improvement of CG by JFET SF.

To address these topics, 8 major variations of jots are tested: (1) TPG jot with SC MOSFET SF; (2) TPG jot with BC MOSFET SF; (3) PTR jot with SC MOSFET SF; (4) PTR jot with BC MOSFET SF; (5) TPG jot with SC JFET SF; (6) TPG jot with BC JFET SF; (7) PTR jot with SC JFET SF; and (8) PTR jot with BC JFET SF. Each type of jot also contains several small variations in the layouts and the implantations. Note that all the jots use a 2-way shared readout architecture and have a pitch size of 1.1μm, and all of them use the pump-gate technique. As shown in Fig. 1, the pump-gate jot doping profile is adopted from the previously demonstrated design and optimized for an improved effective fill-factor and better response in the shorter wavelength regime.

The design of the JFET SF is shown in Fig. 2. More details of this device can be found in [6]. In this device, the FD is also the gate of the JFET. The channel is p-type, and the potential of the gate modulates the channel cross-section depletion area and thus controls the voltage on the source. When the source is biased by a constant current source, the device works as a source follower. The JFET SF can effectively reduce the FD parasitic capacitance induced by the SF gate, hence improve the CG. On the other hand, it can reduce the interaction between the channel carriers and the surface interface traps, which is widely believed to be the major source of the SF 1/f noise and RTS noise [7, 8]. From these two aspects, the reduction of read noise is expected.

In Fig 3, the doping profile of a PTR diode is shown. To further improve the CG, the PTR diode is used to eliminate the overlap capacitance between the FD and the reset gate (RG). In this device, the FD is reset by applying a relatively high voltage on the reset drain (RD) node. As the depletion region of the RD extends to the FD, the "punch-through" occurs. A current path is created under this condition and the reset can be completed. Except for the reset phase, the RD is biased to a relatively low voltage to maintain a potential barrier between the FD and the RD, which prevents the current flow between the two terminals. More design considerations about this device can be found in [6]. The initial PTR technique was developed by Kodak in 1996 to eliminate the reset noise and to achieve a faster global reset over the entire array of pixels [9]. Recently, it was also applied to improve the CG of CMOS image sensor (CIS) pixels. It is worth noting that because of the high full-well capacity (FWC) required by CIS, a high operating voltage (25V) is needed for a proposed PTR device, as suggested in [10]. Since the high voltage is hard to fit the regular CMOS process, the application is constrained. Recently, a bootstrapping technique was proposed to reduce the voltage needed for the gateless reset, and an improved CG of 172μV/e- was achieved [11]. The PTR is a perfect fit for QIS applications due to the small FWC needed by jots. The implementation of PTR technique in QIS started in 2015 at Dartmouth [12], and the PTR diode for QIS can accomplish the reset process with a much lower voltage (e.g. 2.5V).

III. Characterization Results

A simplified schematic of the analog readout chain is shown in Fig. 4. In the readout unit, each column of jots is connected to a correlated double sampling (CDS) circuitry. Every 4 CDS units share one unity-gain buffer. The buffered signal is then amplified by a switched capacitor programmable gain amplifier (PGA). In the testing, a gain of 10 was used to get the optimal noise performance. After the PGA, another unity-gain amplifier is used to drive the output pad. To suppress the noise in the subsequent readout electronics, correlated multiple sampling (CMS) was used, where 20 serial CMS cycles were performed for each read. It was found that more cycles could not further reduce the read noise, probably because of the addition of low-frequency noise due to the extended sampling duration.

The CG and read noise were characterized with the photon counting histogram (PCH) method [13]. In this measurement, the PCH of each jot was created from 20k continuous reads. The read noise was extracted from the valley-peak-modulation (VPM) by fitting the PCH to an analytic Poissonian-Gaussian model, and the CG was extracted from the peak-to-peak distance. Due to a limited functionality of the testing board and the large number of samples needed for PCH, it is time-consuming to measure the PCH for all the jots, so about 7k jots of each type were tested. The inevitable variability in the fabrication process leads to performance variation among devices. For example, small misalignments of masks may lead to the variation of CG, and the randomness in the number of defects and interface traps in each jot may lead to different voltage-referred noise. The histograms of the output-referred CG (after in-jot SF) are shown in Fig. 5. A 2-3% variation of CG is observed in the jots with MOSFET SF. Among the shown 4 types of jots, because of the further reduction of the FD capacitance, the CG of the PTR jots is about 10% higher than the TPG jots (~370μV/e- over ~340 μV/e- in average). Note that the type of the MOSFET SF (BC or SC) has a negligible impact on the CG, which suggests that the two types of SF have a similar gain.

The histograms of read noise are shown in Fig. 6. Thanks to the higher CG, the PTR jots also have lower read noise compared to the TPG jots (0.21e- r.m.s. over 0.23e- r.m.s. in average). Among the 14k tested PTR jots (BC or SC), several best-performing "golden" jots with 0.17e- r.m.s. read noise were discovered. The PCH of which is shown in Fig. 8. Note that a relatively long tail can be observed in the read noise distribution, and the jots on the tail were found to have stronger high-frequency noise. Further investigation is needed to conclude the source of the extra noise, but the suspicion is the RTS noise induced by interface traps. Note that both the BC and SC SF showed similar noise performance, so the effectiveness of noise reduction from the BC MOSFET SF is weaker than expected. The scatter plots of CG versus voltage-referred read noise are shown in Fig. 7. The plots suggest that the variation of read noise and CG have a minimal correlation.

The SC JFET was discovered to have very low SF gain due to a weak control of the channel current by the gate voltage. The suspected reason is that there are some current leakage paths between the source and drain through the silicon substrate. The BC JFETs have a higher SF gain. However, a large variation in operating voltages was found among devices. The variation makes it challenging to do the simultaneous measurement for multiple jots, and manual adjustment was needed for the testing. Hence, individual jots were tested selectively based on their response to the light. Some JFET jots demonstrated significantly improved CG. As shown in Fig. 10, the PTC of one JFET showed 540μV/e- CG, and read noise of 0.34e- r.m.s. was demonstrated with PCH (Fig. 9). The PTC of the JFET also reflected a relatively small linear gain region as it works as a SF, which leads to a concern of the uniformity over multiple devices. The voltage-referred read noise from JFET is unexpectedly higher than MOSFET, which competes with the improvement obtained from the CG. The voltage noise spectrums of the JFET SF and the MOSFET SF are compared in Fig. 11. As shown, 1/f noise is the dominant noise type in all the compared devices. The 1/f noise is widely believed to be caused by the interface traps, the fluctuation in the number of carriers, and the fluctuation of the carrier mobility. The JFET showed similar noise to the MOSFET in the high-frequency region ($>10^5$Hz), where the noise is likely dominated by the RTS noise from interface traps. Hence, we believe the interface traps are not the reason for the high voltage noise from the JFET. On the other hand, the JFET showed higher noise in the low-frequency region. There are no evident causes so far, but a rational suspicion is a relatively high fluctuation in the number of carriers due to some small current leakage paths. Given the high CG of the JFET jots, its potential to reduce the read noise is still promising. More investigation will be done on the origins of 1/f noise, and necessary design modifications will be made to improve the performance of the JFET jots in the future.

IV. Summary

In this paper, the concept and design of multiple new QIS jot devices are introduced. Each device is experimentally demonstrated in a 1Mjot QIS. The performance of them is discussed, with an emphasis on the comparison of the noise performance between different types of SF.

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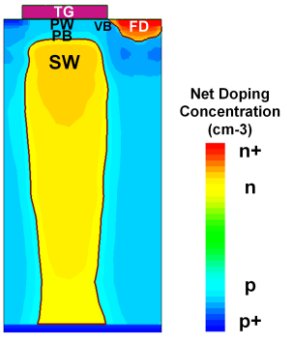

Figure 1: Doping profile of the pump-gate jot from TCAD simulation.

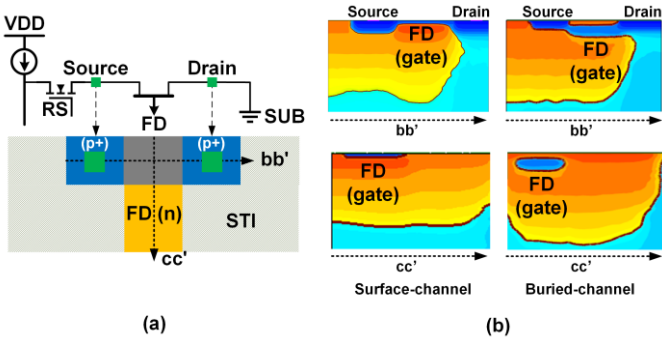

Figure 2: (a) Simplified layout of and schematic of the JFET SF. (b) Doping profile of the buried-channel and surface-channel JFET SF from TCAD

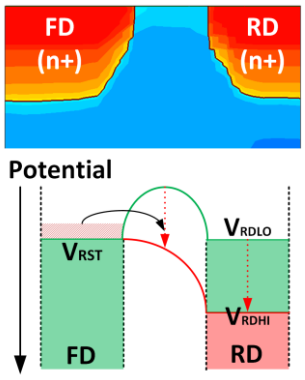

Figure 3: Doping profile of the punch-through reset diode from TCAD simulation and its operation diagram.

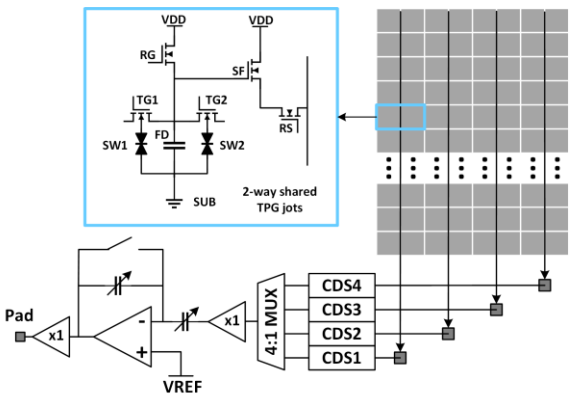

Figure 4: Simplified schematic of one on-chip readout unit.

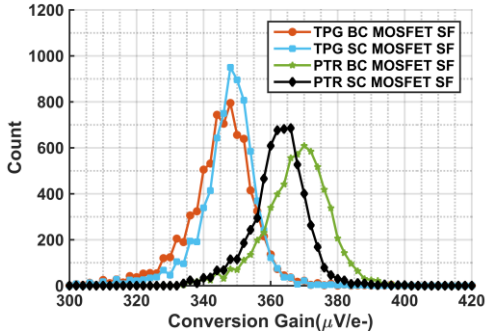

Figure 5: Histograms of CG for TPG and PTR jots.

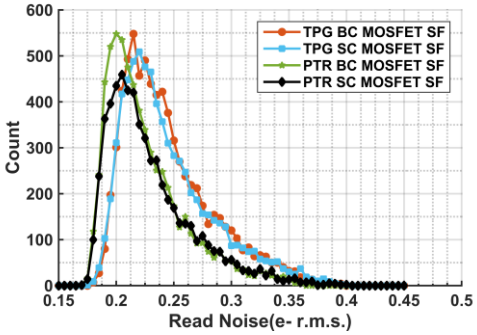

Figure 6: Histograms of read noise for TPG and PTR jots.

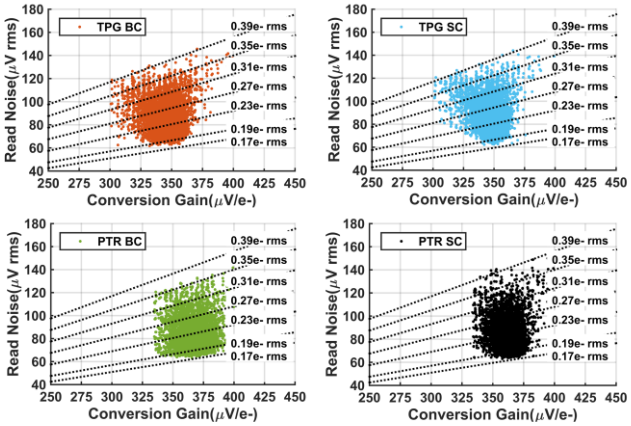

Figure 7: Scatter plot read noise vs. CG for TPG and PTR jots.

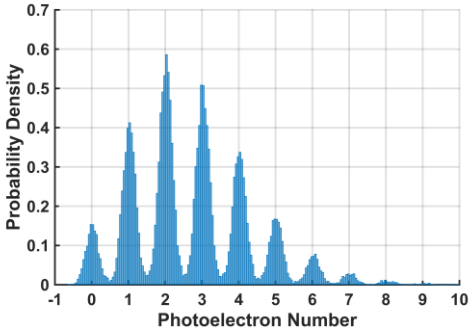

Figure 8: PCH for a "golden" PTR jot with 0.175e- r.m.s. read noise for a mean signal of 2.15e-.

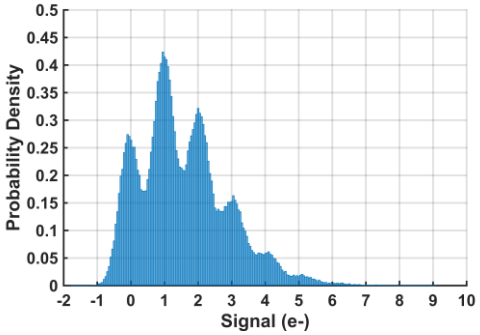

Figure 9: PCH for a JFET jot with 0.34e- r.m.s. read noise for a mean signal of 1.56e-.

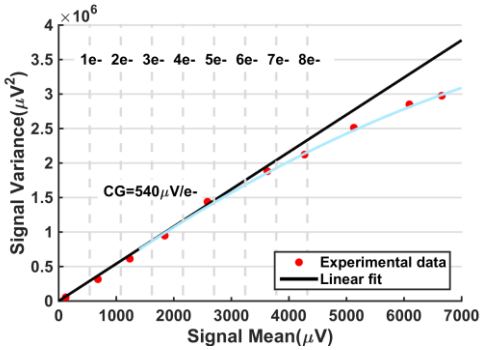

Figure 10: PTC for a JFET jot with 540μV/e- CG.

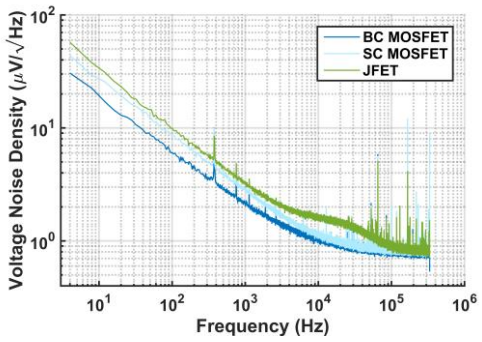

Figure 11: The comparison of the voltage noise density among the jots with a BC MOSFET SF, a SC MOSFET SF and a JFET SF.

Table 1: Jots Characterization Results

	TPG SC	TPG BC	PTR SC	PTR BC	JFET
CG Mean (μV/e-)	347.2	345.1	362.5	367.8	540.0
CG Var.[1]	2.91%	2.56%	2.23%	2.59%	TBD
Read Noise Mean @ RT (e- r.m.s.)	0.235	0.236	0.219	0.216	0.340
Read Noise Variation[1]	16.3%	15.7%	16.3%	15.3%	TBD
SF Noise (μV r.m.s.)	81.6	81.4	79.4	79.4	183.6
Dark Current @RT	0.1e-/sec/pix (1.32pA/cm²)				TBD
Process	TSMC 45nm/65nm stacked BSI				
Pixel Pitch	1.1μm				
Readout	2-way shared readout				

[1] variation stands for the ratio of standard deviation over mean